In The Claims:

For the Examiner's convenience, all claims are presented herein. Please amend claims 1, 5-6, 9, 13, 15-19, 22, 29, and 31-33 as indicated below.

Presentation Of The Claims In A Clean-Unmarked Format

1. (Five Times Amended) A system comprising:

an instruction memory to store a plurality of predefined bus stimuli instructions, the predefined bus stimuli instructions representing a plurality of bus transactions; and

one or more phase generators coupled with a bus and the instruction memory, the one or more phase generators to drive a series of signals on the bus corresponding to the predefined bus stimuli instructions in a predefined sequence.

3. The system of claim 1, wherein the instructions comprise instruction words having a predefined length.

4. The system of claim 1, wherein the one or more phase generators are further responsive to signals received from the bus.

5. (Three Times Amended) The system of claim 1, further comprising a response memory coupled with the phase generator to store predefined responses to signals received from the bus.

6. (Three Times Amended) The system of claim 1, wherein the at least one of the one or more phase generators includes at least one digital logic device responsive

to the instructions and at least one phase engine to control timing of the bus stimuli.

7. The system of claim 6, wherein the digital logic device comprises a field programmable gate array.

8. The system of claim 6, wherein the digital logic device comprises an application specific integrated circuit.

9. (Two Times Amended) The system of claim 6, wherein the at least one digital logic device includes a control portion to provide bus control signals and a data portion to send data to the bus.

10. The system of claim 9, wherein the control portion includes a flow logic device, a request logic device, and a data logic device.

11. The system of claim 6, wherein the at least one phase engine includes at least one logic level translation device.

12. The system of claim 6, wherein the at least one phase engine comprises a system phase engine, an arbitration phase engine, a request phase engine, a snoop/error phase engine, and a data phase engine.

13. (Two Times Amended) The system of claim 9, further comprising a data memory coupled with the data portion.

14. The system of claim 9, wherein the data portion further receives data from the bus.

15. (Four Times Amended) A system comprising:

an instruction memory to store a predefined sequence of bus stimuli representing a plurality of bus transactions;

a flow logic device responsive to the instruction memory;

a request logic device responsive to the instruction memory;

a data logic device responsive to the instruction memory;

a data memory coupled with the data logic device to store data to be exchanged with agents on a bus;

a system protocol generator coupled with the bus and the flow logic device;

an arbitration protocol generator coupled with the flow logic device and the bus;

a request protocol generator coupled with the flow logic device, the request logic device and the bus;

a snoop/error protocol generator coupled with the request logic device and the bus;

a data protocol engine coupled with the data logic device; and

a transaction response memory coupled with the flow logic device and the request logic device to store digital data representing predefined responses to signals received from the bus.

16. (Four Times Amended) A system comprising:

a first means to store instructions representing a plurality of predefined bus transactions; and

second means to drive the plurality of predefined bus transactions as signals on the bus.

17. (Two Times Amended) The system of claim 16, further comprising third means to store data representing predefined responses to signals received from the bus, and

wherein the second means implements the predefined responses based on the signals received from the bus.

18. (Two Times Amended) The system of claim 16, further comprising fourth means to control the timing of the signals provided to the bus by the second means.

19. (Two Times Amended) The system of claim 16, further comprising fifth means to store data to be exchanged with agents on the bus, wherein the second means transmits data from the fifth means in response to the instructions stored in the first means.

20. The system of claim 19, wherein the second means further receives data from the bus and stores the data in the fifth means.

21. A method for testing a bus comprising:
receiving instruction words corresponding to predefined bus stimuli, the predefined bus stimuli representing a plurality of bus transactions; and
executing the plurality of bus transactions by converting the instruction words to signals and driving the signals on the bus.

22. (Three Times Amended) The method of claim 21, further comprising:
defining a sequence of desired bus transactions; and
assembling the sequence of desired bus transactions into instruction words wherein the sequence of bus transactions are executed when the instruction words are converted to signals and driven on the bus.

23. The method of claim 21, further comprising providing predefined signals to the bus in response to signals received from the bus.

24. The method of claim 21, further comprising exchanging data with agents on the bus.

29. (Amended) A system comprising:

an instruction memory to store a plurality of predefined bus stimuli instructions, the predefined bus stimuli instructions representing signals associated with a plurality of bus transactions on a bus;

at least one phase generator coupled with the bus and the instruction memory, the at least one phase generator to provide signals to the bus corresponding to the predefined bus stimuli instructions.

E8

30. The system of claim 29, wherein the predefined bus stimuli instruction also represents the manner in which the signals are to be transmitted.

31. (Twice Amended) A method comprising:

generating a plurality of instruction words corresponding to a predefined sequence of bus transactions;

storing the instruction words in a memory; and

executing the bus transactions by converting the plurality of instruction words into signals and driving the signals onto the bus in the predefined sequence.

E9

32. (Amended) The system of claim 1, further comprising:

an interface other than the bus coupled with the instruction memory, the interface to connect with a device to receive a plurality of predefined bus stimuli instructions.

E10

33. (Amended) The system of claim 1, wherein the plurality of predefined bus stimuli instructions are to drive a predefined ordered sequence of bus transactions onto the bus.